



VLSI PHYSICAL DESIGN

PROF. INDRANIL SENGUPTA

Department of Computer Science and Engineering
IIT Kharagpur

TYPE OF COURSE : Rerun | Elective | UG/PG

COURSE DURATION : 12 weeks (24 Jan' 22 - 15 Apr' 22)

EXAM DATE : 24 Apr 2022

PRE-REQUISITES : Basic concepts in digital circuit design

INTENDED AUDIENCE : Computer Science and Engineering / Electronics and Communication Engineering / Electrical Engineering

INDUSTRIES APPLICABLE TO : Intel, Cadence, Mentor Graphics, Synopsys, Xilinx

COURSE OUTLINE :

The course will introduce the participants to the basic design flow in VLSI physical design automation, the basic data structures and algorithms used for implementing the same. The course will also provide examples and assignments to help the participants to understand the concepts involved, and appreciate the main challenges therein.

ABOUT INSTRUCTOR :

Prof. Indranil Sengupta has obtained his B.Tech., M.Tech. and Ph.D. degrees in Computer Science and Engineering from the University of Calcutta. He joined the Indian Institute of Technology, Kharagpur, as a faculty member in 1988, in the Department of Computer Science and Engineering, where he is presently a full Professor. He had been the former Heads of the Department of Computer Science and Engineering and also the School of Information Technology of the Institute. He has over 28 years of teaching and research experience. He has guided 22 PhD students, and has more than 200 publications to his credit in international journals and conferences. His research interests include cryptography and network security, VLSI design and testing, and mobile computing.

COURSE PLAN :

- Week 1:** Introduction to physical design automation
- Week 2:** Partitioning, Floorplanning and Placement
- Week 3:** Grid Routing and Global Routing
- Week 4:** Detailed Routing and Clock Design
- Week 5:** Clock Routing and Power/Ground
- Week 6:** Static Timing Analysis and Timing Closure
- Week 7:** Physical Synthesis and Performance Driven Design Flow
- Week 8:** Interconnect Modeling and Layout Compaction
- Week 9:** Introduction to Testing, Fault Modeling and Simulation
- Week 10:** Test Pattern Generation, DFT and BIST
- Week 11:** Low Power Design Techniques
- Week 12:** Low Power Design Techniques (contd.)