SYNTHESIS OF DIGITAL SYSTEMS

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TYPE OF COURSE	:	Rerun	Elective	UG
COURSE DURATION	:	12 weeks (29 Jul'19 - 18 Oct'19)
EXAM DATE	:	17 Nov 2019

PRE-REQUISITES	:	Digital Design (or Logic Design), Data Structures
INDUSTRY SUPPORT	:	Synopsys, Cadence Design Systems, Mentor Graphics, Intel, NXP, IBM

COURSE OUTLINE

This course is about the automatic generation of digital circuits from high-level descriptions. Modern electronic systems are specified in Hardware Description Languages and are converted automatically into digital circuits. We will introduce the VHDL Hardware Description Language, and follow it up with a discussion of the basics of synthesis topics including High-level Synthesis, FSM Synthesis, Retiming, and Logic Synthesis.

ABOUT INSTRUCTOR

Prof. Preeti Ranjan Panda received his B. Tech. degree in Computer Science and Engineering from the Indian Institute of Technology Madras and his M. S. and Ph.D. degrees in Information and Computer Science from the University of California at Irvine. He is currently a Professor in the Department of Computer Science and Engineering at the Indian Institute of Technology Delhi. He has previously worked at Texas Instruments, Bangalore, India, and the Advanced Technology Group at Synopsys Inc., Mountain View, USA, and has been a visiting scholar at Stanford University. His research interests are: Embedded Systems Design, CAD/VLSI, Post-silicon Debug/Validation, System Specification and Synthesis, Memory Architectures and Optimisations, Hardware/Software Codesign, and Low Power Design.

COURSE PLAN

Week 1 : Course Outline and Introduction to VLSI Design Automation

Week 2 : Hardware Description Languages and VHDL

Week 3 : Specifying Behaviour and Structure in HDL

Week 4 : Introduction to High-level Synthesis

Week 5 : Compiler Transformations in High-level Synthesis

Week 6 : Scheduling

Week 7 : Register Allocation and Timing Issues

Week 8 : Finite State Machine Synthesis

Week 9 : The Retiming Problem

Week 10 : Introduction to Logic Synthesis and Binary Decision Diagrams

Week 11 : Two-level and Multi-level Logic Optimisation

Week 12 : Technology Mapping, Timing Analysis, and Physical Synthesis